REMARKS

The present Amendment does not add, cancel, or amend any claims. Accordingly, claims 1-5, 7-9, 17-21, 23, 24, and 26-30 remain pending in the application. Claims 1, 17, 24, and 26 are independent.

In the office action, the Examiner (1) indicated that the application contained claims that were drawn to a non-elected invention, (2) rejected Claims 1-5, 7-9, 17-21, 23, 24, and 26-30 under 35 U.S.C. § 103(a) as being unpatentable over "Applicants' Admitted Prior Art (AAPA) in view of U.S. Patent No. 6,211,608 issued to Raina et al. ("Raina"), U.S. Patent No. 5,534,743 issued to Jones et al. ("Jones '743"), and U.S. Patent No. 6,069,443 et al. ("Jones '443"), (3) rejected Claims 6, 22, and 31 under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Raina, Jones '743, Jones '443 and further in view of U.S. Patent No. 5,578,896 issued to Haung et al. ("Haung"). Reconsideration and allowance of the application, are requested.

I. Election/Restriction requirement

The Examiner indicates that the application contains claims 10-16 and 25 drawn to an invention nonelected without traverse. Further, the Office Action indicates that a complete reply must include cancellation of non-elected claims or appropriate action.

Applicants have previously responded to a Restriction Requirement wherein claims 10-16 and 25 were withdrawn from consideration. Additionally, the Office Action dated May 12, 2003 specifically acknowledges withdrawal of claims 10-16 and 25 from consideration. Applicant therefore respectfully request withdrawal of this requirement, as appropriate action has already been taken and acknowledged by the Office.

II. § 103(a) Rejections

The Examiner rejected Claims 1-5, 7-9, 17-21, 23, 24 and 26-30 under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view Raina, Jones '743, and Jones '443. The Examiner states that the AAPA differs from the claimed invention in that a separately deposited insulator layer is disposed between the resistive layer and the dielectric structure. The Examiner

contends that Raina discloses that resistive layers tend to have pinholes causing shorts to develop, and teaches the formation of a buffer layer insulator to substantially eliminate the possibility of short-circuiting via the resistive layer. The Jones references are cited for disclosing that multiple insulative layers can be used to avoid short circuiting due to pin hole defects. The Examiner further contends that by providing multiple layers, the possibility that pinhole defects might line up to cause a short circuit is minimized. Additionally, the Examiner indicates that the order of the layers is immaterial, so long as the net effect is to electrically isolate the cathode from the gate electrode. These rejections are respectfully traversed.

Raina discloses an FED having a buffer layer 58 between an overlying resistor layer 60 and an underlying cathode conductive layer 56 (as shown in Fig. 8 of the reference). The buffer layer 58 is used so that pinhole defects that extend through the resistor layer 60 terminate at the buffer layer 58 without reaching the cathode conductive layer 56. Accordingly, the buffer layer 58 is positioned between the resistor layer and the cathode conductive layer 56. In addition, the buffer layer 58 completely covers the top and sides of the cathode conductive layer 56 that face the resistor layer 60. In particular, the buffer layer is provided to prevent the possibility of short circuit between electron tips and the gate electrode. Column 9, lines 48-67.

Claim 1 of the present application is directed to a method of making a cathode assembly of an FED, which includes forming an emitter electrode structure on the substrate; forming a resistive layer over the emitter electrode structure; and forming an insulative layer on a portion of the resistive layer. Thus, an insulative layer is formed on a portion of a resistive layer, which in turn is formed over the emitter electrode structure. As indicated in the specification (e.g., on page 8) a significant purpose of the insulative layer is to reduce the possibility of shorting between the addressing column line and the row line structure, which shorting might result, e.g., from intrinsic defects in the dielectric structure or unintended variations in spacing between the substrate and grid surfaces.

Contrary to the claimed invention, Raina is not concerned with preventing short-circuiting between the column and/or line row structures. Raina neither acknowledges nor discusses the problems addressed by the present invention. Applicant disagrees with the

Examiner's contention that the order of the layers is immaterial. The order of the layers relates to the problem being addressed. Raina would not have considered layers arranged according to the method defined by claim 1 because such an arrangement would not resolve the problem addressed by Raina, namely to prevent short-circuiting between the emission tips and the gate electrode. Additionally, Raina's buffer layer could not be applied to the FED of the present invention for purposes of preventing short-circuiting between the row line structure and the column line structure. This contention amounts to nothing more than hindsight reasoning, which has been repeatedly held to be improper and impermissible.

Raina only discloses a buffer layer positioned between the resistor layer and the cathode conductive layer 56. It does not suggest placing the buffer layer on the resistor layer because that would defeat the purpose of the buffer layer, which is to protect the cathode conductive structure from pin holes in the resistor layer. Therefore, even assuming that AAPA is properly combinable with Raina, the combination would, at best, only teach that a buffering layer be placed between the emitter electrode structure on the substrate and the resistive layer on the emitter electrode structure of AAPA. One skilled in the art would find no suggestion or have any incentive for placing the buffering layer on a portion of the resistive layer. That, in fact, would defeat the purpose of the buffering layer, which is to protect the cathode conductive structure from pin holes in the resistor layer as noted above. Thus, the cited prior art teaches away from the combination suggested by the Examiner. The cited Jones and Huang references add nothing further in this regard. Therefore, Claim 1 and dependent Claims 2-9 are patentable over the cited references. The remaining pending claims are similarly allowable.

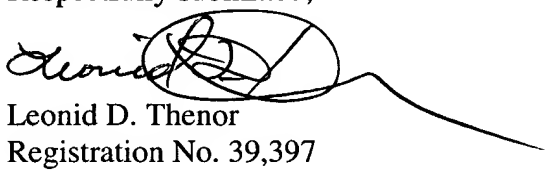
Claims 1-9, 17-24 and 26-31 are pending in the present application. As the application is now believed to be in condition for allowance, issuance of a Notice of Allowance is respectfully requested.

AUTHORIZATION

The Commissioner is hereby authorized to charge any additional fees that may be required for this Response, or credit any overpayment, to deposit account number 08-0219.

In the event that an extension of time is required, or which may be required in addition to that requested in a petition for an extension of time, the Commissioner is requested to grant a petition for that extension of which is required to make this response timely, and is hereby authorized to charge any fee for such, to deposit account number 08-0219.

Respectfully submitted,



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Date: **April 29, 2004**

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